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EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,432	RUPLEY ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-22 have been examined.

Acknowledgment of papers filed: oath and specification on July 31, 2003 and drawings on February 17, 2004. The papers filed have been placed on record.

Specification

The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner asks that the different sizes of rename registers be mentioned. The title is suggested to be changed to "Apparatus and Method Using Different Size Rename Registers for Partial-bit and Bulk-bit Writes".

The disclosure is objected to because of the following informalities: In paragraph 68, table 1, #5, 2nd last line, "appropnate" should be changed to "appropriate".

Claim Objections

2. Claim 9 is objected to because the use of the limitation "n" which is used prior in claim 2. The examiner does not believe that the number of bits in the logical register is equal to the number of rename registers. This is not supported by the specification.

For the purpose of examination, the examiner assumes that the limitation "n" in claim 9 is different from that in claim 2. The examiner requests that the limitation be changed.

3. Claim 14 is objected to because the limitation "written in accordance with any of a plurality of access types" is followed by the limitation "the plurality of access types including: a partial-bit write of 1 bit position; a bulk-bit write of x bit positions..." It is unclear as to whether the register can be written in accordance with any access type, or it is somehow limited by the specific access types listed. For the purpose of examination, the examiner assumes the claim is not limited by the examples of access types. Also, the examiner assumes that the method includes writing a bulk-bit write of x bit positions in order to be able to examine dependant claims which depend on this limitation. Further, claim 14 recites the limitation "the destination register" in line 8. There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination, the examiner assumes the limitation to be "a destination register".

4. Claim 17 is objected to because it recites the limitation "the y bit positions". There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination, the examiner assumes claim 17 is dependant on claim 16 instead of claim 14.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-8, and 14- 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Eickemeyer (U.S. Patent No. 6,393,552 B1).

7. Regarding claim 1, Eickemeyer discloses an apparatus comprising: a storage structure to store at least one entry (fig. 3, ref. 313), the at least one entry to include a register identifier value (fig, 3, ref. 335; col. 4, lines 53-57); a first physical rename register of a first length (fig. 3, ref. RR1A; col. 3, lines 55-60); and a second physical rename register of a second length different than the first length (fig. 3, ref. RR1; col. 3, lines 55-61); wherein the register identifier value is to indicate a current length, wherein the current length is selected from a set including the first length (64 bits, RR1) and the second length (32 bits, RR1A) (col. 4, lines 27-39 & 53-57).

Note that if both status bits are set, the processor renames using the RR1 register (which is 64 bits long); otherwise, it uses the RR1A register (which is 32 bits long). Further note that the registers RR1 and RR1A do share common bits, however, the application does not explicitly claim that the registers cannot share bits.

8. Regarding claim 2, Eickemeyer discloses the apparatus of claim 1, wherein: the first and second rename registers belong to a plurality of n physical rename registers,

wherein n>2; each of the n physical rename registers is of a distinct length; and the set includes each of the n distinct lengths (col. 3, lines 54-61).

Note that the plurality of registers includes all 32-bit registers in the first sector (RR1A-RRnA & RR1B-RRnB) and all of the full 64-bit registers. The two values 32-bit and 64-bit are distinct lengths and all registers of the plurality of physical rename registers are either 32-bit or 64-bit.

9. Regarding claim 3, Eickemeyer discloses the apparatus of claim 1, wherein: the storage structure is to store a plurality of entries, each of the plurality of entries to include a corresponding register identifier value (fig. 3, refs. 331, 333, & 335;).

10. Regarding claim 4, Eickemeyer discloses the apparatus of claim 1, wherein: the first physical rename register is one of a plurality (z) of physical rename registers of the first length (fig. 3, refs. 309 & 311; col. col. 3, lines 54-61).

11. Regarding claim 5, Eickemeyer discloses the apparatus of claim 1, wherein: the second physical rename register is one of a plurality (m) of physical rename registers of the second length (fig. 3, RR1-RRN; col. col. 3, lines 54-61).

12. Regarding claim 6, Eickemeyer discloses the apparatus of claim 4, wherein: the second physical rename register is one of a plurality (m) of physical rename registers of the second length (fig. 3, RR1-RRN; col. col. 3, lines 54-61).

13. Regarding claim 7, Eickemeyer discloses the apparatus of claim 6, wherein: z is not equal to m.

Note that for each 64-bit register there are two 32-bit registers, therefore z and m are not equal.

14. Regarding claim 8, Eickemeyer discloses the apparatus of claim 1, further comprising: a logical register (fig. 3, AR1); and rename logic to map an instance of the logical register to a selected physical rename register, where the selected physical rename register is selected from a plurality of registers comprising the first physical rename register and the second physical rename register (col. 3, lines 54-61).

Note that the logical register AR1 can be mapped to any of the rename registers RRN if the entire 64 bits need to be mapped or any of the registers RRNA if only 32 bits need to be mapped.

15. Regarding claim 14, Eickemeyer discloses a method comprising: determining if a current instruction indicates a multiple-bit-field (MBF) register (col. 4 lines 39-45)

Note that if the register being renamed modifies the entire register, it will use the entire rename register (MBF, RR1; see above regarding claim 1)

Having n bit positions, where n>1 (n = 64; note that it is apparent that Eickemeyer intended "entire 64-bit register, the 8 bytes" on col. 4, lines 40-41; see col.

3, line 45 & col. 4 line 22); wherein the MBF register is to be written in accordance with any of a plurality of access types (col. 4, lines 21-32);

Note that if an instruction uses an entire 64-bit register, it is considered to be an instruction that indicates a multiple-bit-field register that has n (64) bit positions. Note also that the plurality of access types include all access types. Therefore all instructions would fall into the plurality of access types.

A bulk-bit write of x bit positions, where $1 < x \leq n$ ($x = 64$; col. 4, lines 21-32);

Note that the partial-bit write is a 1 sector write of 32 bits (one sector) and the bulk-bit write is a 2-sector write of 64 bits.

Allocating (renaming; col. 4, lines 23-25) a physical rename register (fig. 3, RR1 or RR1A; col. 4, lines 4-46) for a destination register (fig. 3, AR1; col. 4, lines 4-46); wherein allocating further comprises allocating a physical rename register of a first length (RR1A, length = 32) if the current instruction indicates a partial-bit write (col. 4, lines 39-43) and further comprises allocating a physical rename register of a second length (RR1) if the current instruction indicates a bulk-bit write (col. 4, lines 43-46).

Note that the examiner considers a partial-bit write to be a write of one sector of a register and a bulk-bit write is considered to be a two-sector write.

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16. Regarding claim 15, Eickemeyer discloses the method of claim 14, wherein: allocating further comprises modifying a rename map table to indicate the allocated physical rename register (fig. 3, ref. 313; col. 4, lines 7-13).

17. Regarding claim 16, Eickemeyer discloses the method of claim 14, wherein: the plurality of access types further includes a partial-bit write of y bit positions, where 1<y<x (see above regarding claim 14).

Note that the partial-bit write of y bit position is the write to one sector of the register file (32 bits).

18. Regarding claim 17, Eickemeyer discloses the method of claim 16, wherein: the y bit positions are contiguous (see above regarding claim 14).

Note that if one sector is written, all bits of the sector are contiguous.

19. Regarding claim 18, Eickemeyer discloses the method of claim 14, wherein: the x bit positions are contiguous.

Note that the bit positions are contiguous because the bits are the entire register.

20. Regarding claim 19, Eickemeyer discloses the method of claim 14, wherein: the plurality of access types includes a bulk-bit write of all n bit positions (see above regarding claim 14).

21. Regarding claim 20, Eickemeyer discloses the method of claim 16, wherein: y=2.

Note that if the instruction writes 16 bits, the instruction must also write 2 bits and another 14 bits.

22. Regarding claim 21, Eickemeyer discloses the method of claim 16, wherein: y=4.

Note that if the instruction writes 16 bits, the instruction must also write 4 bits and another 12 bits.

23. Regarding claim 22, Eickemeyer discloses the method of claim 14, further comprising: modifying the current instruction to indicate the allocated physical rename register in place of the MBF register (fig. 3, ref. 313; col. 4, lines 7-13).

Note that the rename table entry is considered to be part of the instruction. According to the American Heritage College Dictionary Fourth Edition, instruction is defined as "A sequence of bits that tells a computer to perform a particular operation." According to this definition, the table entry is considered to be part of the sequence of bits controlling how the processor operates.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eickemeyer (U.S. Patent No. 6,393,552 B1) in view of Intel (Intel Architecture Software Developer's Manual Volume 2: Instruction Set Reference).

Regarding claim 9, Eickemeyer discloses the apparatus of claim 8, wherein: the logical register includes a plurality of n bit positions; all n bit positions may be accessed together responsive to a second instruction; and the rename logic further to allocate the second physical rename register responsive to the second instruction (col. 4, lines 33-36).

Note that if an instruction modifies the entire register, both sectors are written to and the entire rename register is written to (RR1, see above regarding claim 1).

Eickemeyer does not expressly disclose that a selected one of the n bit positions may be accessed individually responsive to a first instruction that indicates the selected bit position and the rename logic is further to allocate the first physical rename register responsive to the first instruction.

Intel teaches individually accessing a selected one (page 3-51, description, first 2 lines) of the n bit positions of the logical register responsive to a first instruction (page 3-51 BTS instruction) that indicates the selected bit position (page 3-51, description, first 2 lines; bit base). Intel also teaches allocating the first physical rename register responsive to the first instruction (page 3-51 BTS r/m16, imm8 instruction).

Note that the BTS r/m16, imm8 instruction only accesses half of the 32-bit register, therefore the rename logic would only need to allocate the first sector (first physical rename register).

By adding the BTS r/m16, imm8 instruction will not substantially change the main architecture of Eickemeyer. Adding another instruction would have been successful with a reasonable expectation of success. Instructions are commonly added to processor architectures without complications.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Eickemeyer to allow a selected one of the n bit positions to be accessed individually responsive to a first instruction (BTS r/m16, imm8 instruction) that indicates the selected bit position as taught by Intel in order to more precisely read and modify registers by selecting a single bit of the register (Intel, page 3-51, first 2 lines of description). It also would have been obvious to have the rename logic allocate the first physical rename register responsive to the first instruction as taught by Intel in order to provide additional effective registers for renaming (Eickemeyer, last 2 lines of the abstract) by accessing only 16 bits of the register (Intel, page 3-51, lines 6-7 of description).

26. Regarding claim 10, Eickemeyer/Intel discloses the apparatus of claim 9, wherein: a subset including y of the n bits may be accessed responsive to a third instruction (Intel page 3-30; AND AX, imm16), where y>1 (y = 16); and the rename logic is further to allocate the first physical rename register responsive to the third instruction.

Note that the AND instruction can bitwise and the AX register wth an 16-bit immediate. This instruction only accesses 16 bits of the EAX register.

27. Regarding claim 11, Eickemeyer/Intel discloses the apparatus of claim 10, wherein: the length of the first physical rename register includes y bit positions (Eickemeyer, col. 2, lines 3-20).

Note that with the combined instruction, all sectors would be 16 bits wide in order to account for the backwards compatibility of 16-bit instructions.

28. Regarding claim 12, Eickemeyer/Intel discloses the apparatus of claim 11, wherein: the entry is further to include a position identifier, the position identifier to indicate a selected one of the y bit positions of the first physical rename register (Eickemeyer col. 4, lines 27-39 & 53-57).

Note that the sector mask bit selects a sector to used for renaming. By selecting the sector, it also selects the first bit of the register. If the sector is selected, the initial bit of the sector is also selected.

29. Regarding claim 13, Eickemeyer/Intel discloses the apparatus of claim 12, wherein: the selected one of the y bit positions of the first physical rename register corresponds to the selected bit position indicated by the first instruction (Intel page 3-45; BT r/m32, imm8).

Note that if the bit being accessed is in the first 16 bits, then only the first sector needs to be renamed, but if the bit being accessed is in the second 16 bits, only the second sector must be renamed. Therefore, the sector mask corresponds to which to the selected bit position.

Conclusion

30. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571)272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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1/27/06

HENRY W. H. TSAI
PRIMARY EXAMINER